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High aspect ratio and large area metallic nanogrids as transparent electrodes on optoelectronic devices

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The authors demonstrate high aspect ratio and large area metallic nanogrids as transparent electrodes with reduced series resistance on GaAs based optoelectronic devices. The fabrication process uses ultraviolet photolithography techniques, pulsed reactive ion etching, and two metallization steps: a vapor deposited contact seed layer and a thickening step by electrodeposition. As a result, a threefold reduction in resistive power losses is achieved with a contact grid transmission comparable to state-of-the-art devices. © 2016 American Vacuum Society. [http://dx.doi.org/10.1116/1.4954229]

I. INTRODUCTION

Front surface electrodes are key elements for high-performance optoelectronic devices such as solar cells and light emitting diodes (LEDs). The transparency and resistivity of the top side contact determine important energy loss mechanisms in these devices. Reducing the device series resistance by increasing the amount of conducting material on top of the device increases the optical losses due to shadowing. Many devices use transparent conductive oxides (TCO) such as indium tin oxide (ITO), which for a typical 110 nm thick layer offers a sheet resistance of 63.6 Ω/sq, with a 93% optical transmission. Leaving aside the high cost and scarcity of indium, and the brittleness of the material, the high optical and electrical losses make ITO unsuitable for the high-performance devices, such as concentrator photovoltaic devices (CPV). These applications use microscale metallic grids instead, which introduces an important feature, the emitter layer resistance, i.e., the voltage drop the electrons suffer in their way from the photogeneration point to the nearest grid finger. The optimal wire width and spacing therefore depend on a number of parameters and technological constraints, and is determined by a compromise between finger resistance (minimized by increasing finger width), emitter or semiconductor resistance (minimized by increasing the number of fingers), and optical shadowing losses (minimized by reducing both the finger width and the number of fingers). In principle, this compromise means that it is not possible to simultaneously reduce the electrical and optical losses.

The emitter resistance represents around 40% of the electrical losses of CPV devices, and as the generated current scales linearly with concentration, these losses are of great importance as concentration increases, limiting the maximum concentration achievable. Maximum achievable concentration determines the ultimate conversion efficiency and the kW h/$ cost; therefore, there is interest in fabricating grids with reduced resistive power losses by proportionally reducing wire width and spacing. Furthermore, recent research in nanoscale metallic grids suggests that scattering and plasmonic effects at the subwavelength scale may enhance light transmission. This would break the previously mentioned compromise between electrical resistance and optical transmission, opening a new path for efficiency enhancement, but such effects are out of the scope of this work.

In comparison with the state-of-the-art, in this work, we demonstrate the fabrication of large area metallic submicron grids with a threefold reduction in resistive power losses without sacrificing optical transmission. This is made possible by a proportional reduction of line width and line spacing, leading to a virtual suppression of emitter resistance losses, as these are proportional to the square of the line spacing.

II. DESIGN OF THE GRID

As stated by Moore, neglecting contact resistance losses, the total fractional power loss (loss/output power) per unit area at the top contact is given by the sum of the grid resistive loss \( L_G \), the emitter resistive loss \( L_E \), and the optical shadowing loss \( L_S \)

\[
L_G = \frac{j}{V} r_G \quad \text{with} \quad r_G = \frac{\rho_M \cdot S}{12 \cdot h_{fg} \cdot w_{fg}}, \tag{1}
\]

\[
L_E = \frac{j}{V} r_E \quad \text{with} \quad r_E = \frac{R_E \cdot S^2}{12}, \tag{2}
\]

\[
L_S = \frac{w_{fg}}{S}, \tag{3}
\]
where \( j \) is the generated current per unit area, \( V \) is the working voltage of the cell, \( r_G \) is the grid resistance per unit area, \( r_E \) is the emitter resistance per unit area, \( \rho_M \) is the metal resistivity, \( S \) is the finger spacing, \( l_f \) is the finger length, \( h_{fg} \) is the finger height, \( w_{fg} \) is the finger width, and \( R_E \) is the semiconductor (emitter) sheet resistance. One can translate these fractional losses to cell efficiency losses by multiplying by the efficiency of the cell.

The total power loss can be minimized by using two sets of perpendicular wires: a set of closely spaced and thin wires to minimize the emitter resistive loss, and a perpendicular set of thick wires (called busbars) with a large spacing to minimize the metal resistive loss. This is in fact the solution typically used for silicon solar cells. For sufficiently small III–V concentrator solar cells, busbars are only needed at the edges of the device, where there is little or no incident light. In such a case, the effective finger length is half of the smallest lateral dimension in the device. For amorphous or organic materials with a high semiconductor sheet resistance, a TCO is typically used as a top contact, but closely spaced nanowires can also be used. Figure 1 presents three representative cases calculated using the parameters in Table I.

A higher metal resistivity has been assumed in Table I for wires thinner than 200 nm due to the increased electron scattering in nanowires. As specified in Table I, this calculation is for a fixed shadowing loss, \( L_s \), different for each system, and hence a fixed relationship between \( w_{fg} \) and \( S \) (organic/amorphous: \( S = 50 \times w_{fg} \); III–V: \( S = 250 \times w_{fg} \); and Si: \( S = 90 \times w_{fg} \)). The higher energy losses at small finger widths are due to finger resistance losses and at large finger widths are due to increased emitter resistive losses.

As seen in Fig. 1, proportionally reducing finger width and spacing of the state-of-the-art CPV solar cells can result in a reduction in the efficiency losses associated with the top contact from 5% to 1%, primarily due to the reduced emitter resistance.\(^{7-14} \) State of the art III–V concentration solar cell devices have an area of 1 mm\(^2\), and their grid consists of 3 \( \mu \)m width and 600 nm height Au fingers arranged in periods of 100 \( \mu \)m, leading to a shadow loss of 3%.\(^{11} \) This shadow factor \( L_s \) is larger than the optimal of Fig. 1 due to higher than optimal metal resistivity because of impurity diffusion in alloyed contacts. A grid resistance of \( r_G = 5.5 \) m\( \Omega \) cm\(^2\) for a 97% transparency is achieved. A common emitter sheet resistance is \( R_E = 500 \) \( \Omega \)/sq; therefore, the emitter resistance represents around 40% of the total cell series resistance.\(^{11} \) Our goal is to substantially reduce power loss due to the emitter resistance while keeping other parameters unchanged; thus, we aim to shorten the distance between fingers by an order of magnitude (2–20 \( \mu \)m). This means that the finger width must be reduced to 400–600 nm which is also an optimum size regarding electrical performance and reliability issues, since narrower fingers would suffer from increased electron scattering and electromigration.\(^{20,21} \)

Standard grid fabrication procedures need to be revised. Annealed Au/Ge/Ni is the most often chosen metallization. During the necessary thermal annealing step in this type of metallization, gold penetrates into the semiconductor forming spikes up to 400 nm deep and results in low metal conductivities due to impurity diffusion into gold.\(^{22,23} \) This forces the use of very thick (300–500 nm) semiconductor contact layers to prevent short-circuits. As the contact layer elimination is normally done by isotropic wet-etching, in order to achieve a good electrical performance, fingers must be considerably wider than twice the contact layer thickness to avoid etch undercutting problems.\(^{11} \) In order to reduce the width, nonpenetrating metallizations need to be used so that the contact layer can be thinned to 40–80 nm. We have chosen Au/Ge/Pd and Cr/Al for n and p type top contacts, respectively.\(^{24-26} \) Electron beam lithography is a powerful technique in the definition of nanometric grids,\(^{27} \) but is restricted to small patterns. As the solar cells are large area devices, the fabrication process must be scalable; therefore, UV lithography techniques such as laser interference lithography (LIL) and contact optical lithography have been used.\(^{28} \) LIL allows for smaller feature sizes at the expense of reduced design flexibility. Typical values of the grids here presented are as follows: width \( w_{fg} = 350 \) nm, height \( h_{fg} = 400 \) nm, and period \( S = 2.3 \) \( \mu \)m for Cu lines defined by LIL and width \( w_{fg} = 550 \) nm, height \( h_{fg} = 600 \) nm, and period \( S = 16.7 \) \( \mu \)m for Au lines defined by contact photolithography. Two-dimensional grids with similar sizes may be defined by contact photolithography as well.

### III. FABRICATION PROCESS

A fabrication procedure based on UV lithography techniques, plasma etching, and a double step metallization was developed to fabricate large area high-aspect ratio nanogrids, i.e., thin and high lines, with reduced series resistance and 97% optical transmission (Fig. 2). Conventional
grid fabrication procedures are based on a lift-off procedure. High resolution resists do not usually have the required height for a clean lift-off, so they can only produce low aspect ratio lines. Consequently, with the aim of producing high aspect ratio and high-resolution nanogrids, we have designed a procedure based on the pattern transfer to a thick SiO$_x$ mask and the electrodeposition of the thick metal through this mask. For narrow lines (<500 nm), the pattern is defined by a combination of two UV lithography/etch steps: a maskless interferometric lithography exposure for the submicron lines, and a conventional masked UV lithography step for the larger scale busbars.

The first step involves plasma enhanced chemical vapor deposition (PECVD) to deposit a thick layer of SiO$_x$ (400–600 nm) to both protect the semiconductor and serve as a mold for the electrodeposition. Then, a 160 nm thick layer of iCON-16, an organic bottom antireflective coating (BARC), was deposited by spin coating and prebaked at 90°C for 90 s. This layer served to planarize the surface prior to resist coating, lead to a better resolution by preventing reflection and standing waves, and serve as a lift-off layer after the contact seed layer deposition. For LIL exposure, a 500 nm thick layer of SPR505A positive photoresist was spun-on and prebaked at 95°C for 90 s on top of the BARC. The exposure for the nanoscale lines used a Lloyd’s mirror interferometric lithography system. A 355-nm laser (third harmonic of a YAG laser source) was used; the power density was adjusted so that a dose of ~120 mJ/cm$^2$ was delivered in about 4000 pulses at 80 Hz. After a postexposure bake, 110°C for 60 s, the pattern was developed in a KOH based developer. The resulting pattern [Fig. 2(a)] consisted of 350 nm wide lines on a 2.5 μm pitch. For patterns defined by contact lithography, a 500 nm thick layer of S1805 photoresist is spun coated and then exposed in a vacuum contact mode with a SUSS Microtec MA6/B6 aligner using the 365 nm Hg line. The total exposure was 20 mJ/cm$^2$ followed by a 45 s immersion in M-319 developer. Then, a 90 nm thick layer of Cr is thermally evaporated, followed by lift-off in acetone to define a negative of the pattern that will act as a hard-mask in the subsequent dry etching step. A defect free lift-off is crucial for the continuity and transparency of the resulting grid. A thinner Cr layer would ease the lift-off although the dry etching removes around 60 nm of Cr and the SiO$_x$ hard mask could be affected in areas of the pattern where it should remain intact. For LIL defined grids, it is necessary to open the busbar areas on the Cr layer. To this end, we do a contact lithography step and Cr etch step with Ce$_2$SO$_4$ + H$_2$SO$_4$ + DI H$_2$O (25 g:25 ml:250 ml). Then, an
ohmic contact is formed by the deposition of a thin layer of metals that will also serve as a seed layer for the electrodeposition [Fig. 2(d)]. Then, reactive ion etching (RIE) in an Oxford Plasmaprobe 80 by means of a CHF₃ plasma is performed to transfer the line and busbar pattern to the surface through the iCON-16 and SiOₓ layers. Due to the deep etching, inhomogeneities arise if it is performed in a single step producing nonvertical walls and different etch rates throughout the surface. To avoid that, a pulsed etch is used with an on/off cycle of 30 s/120 s, with N₂ flow in the first off minute. Figure 2(c) shows a profile of the smooth and vertical trenches after this step. Further details of this plasma etching process are chamber pressure: 5 mTorr, RIE power: 200 W, wafer temperature: 30 °C, and output DC Bias: ~475 V. To prevent structural damage in the semiconductor due to the impact of energetic ions, very accurate etching must be performed. This is accomplished by interferometric control of the SiOₓ layer thickness during the last etching cycles. If necessary, the last few tens of nm are etched by immersion in diluted HF.

The metallization consists of sputtered Ge/Pd/Au (30/10/45 nm) for n type top contacts and thermally evaporated Cr/Au (10/60 nm) for p type top contacts. In order to achieve a subsequent filling of the lines, it was crucial to prevent any metal deposition along the sidewalls. Contacts to semiconductors are typically deposited by e-beam evaporation. Although no previous report on sputtering deposition of Ge/Pd/Au contacts seems to exist on the literature, it has been reported that contact deposition with sputtering can lead to a low contact resistance due to in situ oxide removal and surface cleaning as a consequence of low energy plasma bombardment.

The as-deposited contact was rectifying and became ohmic upon annealing (57 s at 450 °C). The required high annealing temperature might be a consequence of the need to anneal the damage caused by the plasma on the semiconductor surface.

The metal on top of the hard mask was removed by lift-off using the BARC as sacrificial layer. This organic BARC was hardened by the dry-etching process, thus complicating its subsequent removal. Cycles of immersion in hot (275 °C) N-methyl Pyrrolidone for 1 h followed by 3 min of ultrasound shaking and 300 W O₂ plasma cleaning for 10 min were used to remove the BARC. Next, the lines are thickened by a potentiostat controlled electrodeposition step. Cu and Au were chosen due to their high conductivity and process compatibility. Cu is deposited in aqueous solution with 1 M H₂SO₄ and 0.005 M CuSO₄ at −0.062 V versus Ag/AgCl reference electrode for 10 min. Usually, CN⁻ containing solutions are used for gold plating, but in this case, a safer gold sulphite/thiosulphate based solution has been used. Gold filling of trenches is barely found in the literature, and in contrast with typical filling procedures, no additives were used. Gold was electrodeposited at a constant potential of −0.3 V versus Ag/AgCl for 40–60 s using a 0.03 M NaAuCl₄ aqueous solution kept at 60 °C with 220 rpm agitation. Small variations in line parameters (width, resistance) may impact on the nucleation and filling time, so to ensure complete filling we let the lines overflow the trench forming nanomushrooms [Fig. 2(e)]. In the semiconductor industry, the most common method for planarization and excess material removal is the chemical mechanical polishing. In a research lab setting, we found this technique to be too sensitive to particle contamination. Therefore, Ar ion-milling (reactive ion beam etching with a 450 V plasma) at an incidence angle of 65° away from the surface normal was used [Fig. 2(f)]. Finally, the SiOₓ hard mask was etched in diluted HF. The resulting contact grids are shown in Fig. 3.

IV. ELECTRODEPOSITION AND ELECTRICAL CHARACTERIZATION

As trench filling with electrodeposited Cu is a common process by the semiconductor industry, we focused our attention on Au electrodeposition. In order to evaluate the electrical properties of the Au nanogrid, three parameters were measured: contact resistance, electrodeposited continuous film sheet resistance, and electrodeposited grid metal sheet resistance. The contact resistance of the sputtered

![Fig. 3. Resulting grid layouts: (a) 2D inverted square grid fabricated by contact lithography with S = 16.7 μm and wfg = 500 nm. Scale bar is 50 μm. (b) LIL defined array of Cu lines with wLIL = 350 nm, bLIL = 400 nm and S = 2.3 μm. Scale bar is 2 μm. (c) Profile of a single 500 nm width and 600 nm height Au line. Scale bar is 500 nm.](image-url)
Ge/Pd/Au contacts was determined by four probe transmission line measurement measurements. The as-deposited contact was rectifying and became ohmic upon a 57 s at 450°C anneal, reaching an optimum value of $p_{CF} = 1 \times 10^{-6}$ Ω cm² for 57 s at 550°C, which is comparable to state-of-the-art contacts for concentrator photovoltaics. The chosen gold electrodeposition conditions were those presenting the best electrical characteristics for the bulk deposit. Cyclic voltammetry was measured for different gold concentrations in order to determine the optimum deposition voltage range for each case (Fig. 4).

Various thick films (>1 μm) within the optimum range were deposited and inspected by x-ray diffraction and SEM to ensure homogeneous coverage and deposit quality. A resistivity of $\rho_M = 3 \times 10^{-8}$ Ω m for the 600 nm electrodeposited Au film was measured by the four probe method. This is comparable to tabulated values for bulk gold. These layers were electrodeposited at 0.03 M NaAuCl₄ concentration and −0.31 V versus Ag/AgCl reference electrode. Finally, the same procedure was done for the grid electrodeposition, since the geometric constraints may affect the deposition conditions. Homogeneous trench filling was achieved for 0.03 M NaAuCl₄ concentration and −0.3 V versus Ag/AgCl, and gold resistivities in the range of $\rho_M = 5–7 \times 10^{-8}$ Ω m are measured, 2–3 times the bulk resistivity. Therefore, for 600 nm high lines (Fig. 3(c)), grid metal sheet resistances of $R_{SG} \approx 85 \, \text{mΩ/sq}$ are achieved, resulting in grid resistances of $r_G = 2 \, \text{mΩ cm}^2$ for contact lithography defined grids with $w_{FG} = 500 \, \text{nm}$, $S = 16.7 \, \mu\text{m}$, and 97% transmission.

These values represent a significant improvement over the $r_G = 5.5 \, \text{mΩ cm}^2$ reported for the same optical transmission by García et al. due to their use of alloyed contacts affected by impurity diffusion into gold. Reducing the finger spacing from 100 to 16.7 μm would represent a 30-fold emitter resistance reduction. On the other hand, obtained values for LIL defined Cu grids shown in Fig. 3(b) are $R_{SG} \approx 0.4 \, \text{Ω/sq}$ and $r_G = 2.3 \, \text{mΩ cm}^2$ for 86% light transmission. Due to the short period of these grids, a 1890-fold reduction in the emitter resistance is expected. Despite the reduction in the resistive losses, the increase in shadowing losses makes these Cu grids less appropriate than state-of-the-art grids.

A highly optimized front contact is a requirement for operation at very high concentrations; therefore, as a reference representative of state-of-the-art front contacts, we have chosen the only solar cell to have attained an efficiency record at a solar concentration higher than 1000 suns due to their use of alloyed contacts affected by impurity diffusion into gold. Reducing the finger spacing from 100 to 16.7 μm would represent a 30-fold emitter resistance reduction. On the other hand, obtained values for LIL defined Cu grids shown in Fig. 3(b) are $R_{SG} \approx 0.4 \, \text{Ω/sq}$ and $r_G = 2.3 \, \text{mΩ cm}^2$ for 86% light transmission. Due to the short period of these grids, a 1890-fold reduction in the emitter resistance is expected. Despite the reduction in the resistive losses, the increase in shadowing losses makes these Cu grids less appropriate than state-of-the-art grids.

V. VEIL FORMATION DURING ION-MILLING

We have found veil-like debris remaining over the GaAs surface after the HF wet etching of the SiOₓ, which might affect dramatically the light transmission. Figure 5 shows SEM images of the veils, which depending on the size, might not be easily observed under the optical microscope (500×)

![Fig. 4. Effect of experimental parameters on electrodeposited gold: (a) a too low concentration of 0.001 M or (b) a too low temperature of 30°C leads to inhomogeneous nucleation and high sheet resistances. Scale bars are 1 μm. (c) Gold electrodeposited at optimal electrodeposition conditions: concentration of 0.03 M and a reference potential of −0.31 V vs Ag/AgCl. The deposit is compact allowing for a low resistivity. Scale bar is 500 nm.](image)

<table>
<thead>
<tr>
<th>Table II. Comparison of the grid parameters and grid related resistances between a CPV state-of-the-art Au grid and the fabricated Au and Cu grids. $S$ is the period, $w_{FG}$ the finger width, $L_S$ the shadow factor, $p_{CF}$ the specific contact resistance, $r_G$ the grid resistance, and $r_E$ the emitter resistance. Significant improvements both in grid resistance and emitter resistances are achieved due to the new geometries and fabrication techniques.</th>
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<td>Grid</td>
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<td>State of the art (Au)</td>
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and sometimes the effect is only perceived as a very slight darkening of the surface. Usually, these structures follow the finger contour but veils crossing over the lines have also been observed, with widths ranging from 10 nm to 2 μm and lengths of hundreds of microns. Such structures might scatter and absorb light heavily, thus reducing photogeneration.

Close SEM inspection of the veils [Fig. 5(a)] suggested that the veils are formed by the mixing of Au and SiOx during ion-milling as was previously reported. Implanted Au atoms prevent SiOx from being etched in HF, so an Au etchant must be added to the HF solution such as KI+I2 which is known to also etch GaAs, but only very slowly at low pH. This step should be performed prior to the SiOx etch, preventing the GaAs device surface from exposure to KI.

As shown in Figs. 5(b) and 5(c), we successfully etched the residual veils using a HF + KI + I2 40:4:1:800 solution in water for 5 min.

VI. SUMMARY AND CONCLUSIONS

We have developed a fabrication procedure for large area and high-aspect ratio metallic grids for use as top electrodes in optoelectronic devices. A thick sacrificial layer (600 nm) of SiOx was deposited by PECVD and serves as mold for metal electrodeposition. After the coating of the resist, lines are defined by LIL and contact UV lithography. A thin layer (90 nm) of Cr deposited by thermal evaporation serves as a hard mask for the dry etching procedure (RIE) to define the pattern on the device surface. Optimum conditions for the pulsed on-off duty cycle of the RIE process have been found to yield vertical and smooth sidewalls. A double step of metallization was used: first, a thin seed layer (90 nm) was deposited by sputtering, and then, the line was thickened (up to 400–600 nm) by means of electrodeposition. Planarization of the metal overflow was achieved by grazing angle ion-milling with Ar, and then, the SiOx mould was etched away with diluted HF with a prior HF + KI + I2 etch to eliminate residues from the ion milling.

Compared to CPV state-of-the-art cell grids with a 3% geometrical shadow factor, a twofold grid resistance reduction and a 30-fold emitter resistance reduction was achieved due to higher metal purity and increased line density, resulting in a threefold reduction of resistive power losses. These results pave the way toward higher concentration and more efficient photovoltaics as well as more efficient and powerful LEDs. Our next efforts, to be reported elsewhere, will be directed to define these grids over state-of-the-art CPV solar cells and evaluate the impact on the conversion efficiency.

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Fig. 5. Veil formation during ion-milling: (a) SEM image of a sample after ion-milling and SiOx etching, showing a single line and the veil in its surroundings. Scale bar is 1 μm. (b) and (c) optical microscope photograph of the same sample region before and after the veil etching in HF + KI + I2. Scale bars are 50 μm.
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